Investigating the Option of Removing Anti-Aliasing Filter From Digital Relays

Sukumar M. Brahma, *Senior Member, IEEE*, Phillip L. De Leon, *Senior Member, IEEE*, and Rajesh G. Kavasseri, *Senior Member, IEEE*

***Abstract*—Digital relays traditionally employ sampling rates less than 100 samples/cycle. In order to avoid aliasing due to fault-transients, these relays employ an analog anti-aliasing filter before critical-sampling (Nyquist rate) the input waveforms coming from instrument transformers. In many applications of Electrical Engineering, oversampling (greater than Nyquist rate) has long been used to simplify the requirements of an anti-aliasing filter with a sharp-cutoff; in some cases the filter can even be eliminated. This paper investigates this option for a digital relay. Performance of a traditional digital relay is compared with a method that uses oversampling without using an anti-aliasing filter. By processing a comprehensive array of fault-waveforms from EMTP simulations, a suitable oversampling rate is suggested. A comparison of phasor estimates using the traditional relay and the proposed method is made for different operating and fault conditions. Results suggest that oversampling can eliminate the anti-aliasing filter traditionally employed in digital relays.**

***Index Terms*—Aliasing, analog to digital converter, discrete Fourier transform, digital relay, power system protection.**

I. Introduction

DIGITAL relays use sampling rates ranging from 8 samples/cycle to as high as 96 samples/cycle [1]. During the inception of a fault, the voltage and current waveforms are superimposed by transients. The amount and duration of transients depend on factors like the instant of fault with respect to the voltage waveform, the type of fault, the location of fault on the line, and the damping available in the system. Faults occurring at instants when the voltage waveform is around its peak value are the most severe in terms of transients. Typically, voltage waveforms experience more severe transients than current waveforms. Digital relays use the discrete Fourier transform (DFT) of the sampled signal to estimate the phasor value of the fundamental. To avoid aliasing, especially during a fault, all digital relays employ an analog (low-pass) anti-aliasing filter before sampling the voltages and currents with a analog-to-digital converter (ADC) [1], [2]. Such a filter introduces a time-delay of 1.5 - 2 ms in the phasor estimation depending on the sampling rate chosen [2]. Such a filter can also be relatively expensive.

In many applications, oversampling, i.e., $f_s \gg 2f_n$, where f_s and f_n are the sampling and Nyquist frequencies respectively has long been used to simplify the requirement of an anti-aliasing filter with a sharp cutoff at f_n. If the oversampling rate is selected such that any aliased frequencies are extremely small or below the noise floor, then the anti-aliasing filter can be made less sharp or in some cases even be eliminated, reducing cost and delay [3]. Many commonly-available ADCs utilize oversampling for these reasons.

Very inexpensive ADC chips are currently available that use oversampling up to a few hundred kHz. Digital music industry today is able to produce excellent sound reproduction by using very simple or no analog pre-filtering in their products. Since adopting inexpensive oversampling can eliminate comparatively more expensive analog filter and the associated time-delay, it is worthwhile to investigate the possibility of removing anti-aliasing filters from digital relays through oversampling. This paper investigates such possibility.

A Power System Relaying Committee (PSRC) report on software-models used in relays indicates that oversampling is used in the newest generation of relays, but the main purpose of oversampling is oscillography [4]. These relays still use an analog anti-aliasing filter and the sampling rate used for phasor estimation is obtained by decimating the data sampled at higher frequency. In our extensive literature search including a patent-search, there is no published document that investigates the phasor-estimation function of a digital relay without using analog pre-filtering.

This paper describes the process where a rationally chosen oversampling rate is tried out on a comprehensive array of fault waveforms generated using Electromagnetic Transient Program (EMTP). Through such trials, we show the phasor estimates using the chosen oversampling rate and without using an anti-aliasing filter are practically the same as the phasor estimates from a conventional digital relay that uses an anti-aliasing filter. Factors like fault type, fault location, fault instant, fault resistance and pre-fault conditions are varied while generating the fault waveforms. Based on the similarity of the phasor estimates for such various conditions, conclusions are drawn to emphasize the effectiveness and feasibility of the proposed approach.

II. Simulation Approach

In order to obtain a preliminary estimate of the required sampling rate to avoid aliasing, the spectral content of the sampled waveform should be measured. In order to perform such spectral analysis, a fault-voltage waveform was obtained using EMTP simulation. A 240-kV, 225-km, two-terminal transmission line with substantially different source

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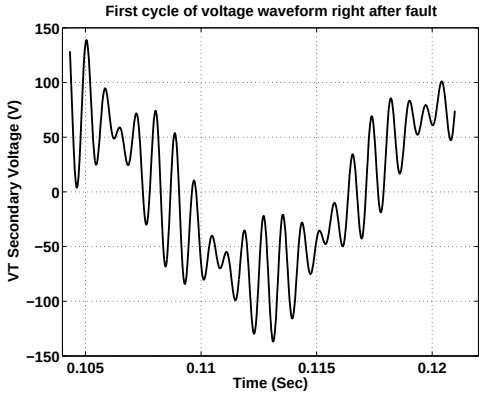
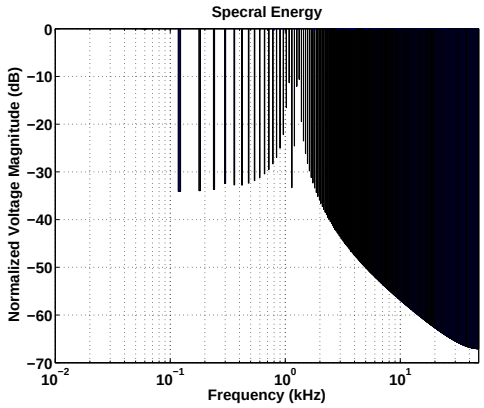


(a)



(b)

Fig. 1. Voltage waveform and its spectral energy using a sampling rate of 96 kHz.

impedances at both ends was simulated on PSCAD/EMTDC® using the long transmission line model. PSCAD/EMTDC® is a time-tested graphical user interface for EMTP with added components. The parameters of the test system are given in the appendix. Load condition was created by a phase angle difference of 15° between the two ends. A line to ground fault on phase A was simulated 50 km from one end, when the A-phase voltage was around its peak. This fault-instant ensures severe transients in the voltage waveform. The A-phase voltage waveform was sampled at an extremely high rate of 96 kHz (1600 samples/cycle) using an appropriate time-step in the simulation. This waveform and its spectral analysis for the first cycle after the fault is shown in Fig. 1 (a) and (b) respectively. The fault instant is 0.1024 seconds in the simulation. Window size spans one cycle, which, in this case, corresponds to 1600 samples. For simplicity, we use a rectangular window and are not averaging the DFT. The DFT is described by:

$$V_h = \frac{2}{N}\sum_{n=0}^{N-1} v(n)e^{-jh2n\pi/N} \quad (1)$$

In (1), V_h is the phasor estimate of the h^{th} harmonic, $N = 1600$, and $v(n)$ is the value of the n^{th} data-sample. Fig. 1 (b) shows the *normalized* voltage magnitude in dB on the Y-axis and the frequency (log-scale) on the X-axis. This means, as can be seen in Fig. 1 (b), the fundamental component (60 Hz) of the voltage waveform has 0 dB magnitude. This form of display provides better comparison of the energy in the harmonics and the energy in the fundamental.

The Nyquist rate for the selected sampling rate of 96 kHz is 48 kHz. Fig. 1 (b) shows the spectral energy up to 48 kHz. If we assume an 8-bit ADC, the signal-to-quantization noise ratio can be approximated as $8 \times 6 = 48$ dB [3]. If the signal of interest spans the full-scale range, as a first order approximation, the aliased components are insignificant based on our observation of the signal-energy beyond 5 kHz. Beyond 20 kHz, the signal energy drops to a very low value. Based on this observation, an oversampling rate of around $2 \times 20 = 40$ kHz should suffice. However, since $f_s = 48$ kHz is a standard sampling rate in audio applications for which very low cost ADCs are widely available, an oversampling rate of 48 kHz was selected. With this sampling rate, the harmonics beyond 24 kHz will be aliased. Clearly, from Fig. 1 (b), such harmonics are almost non-existent.

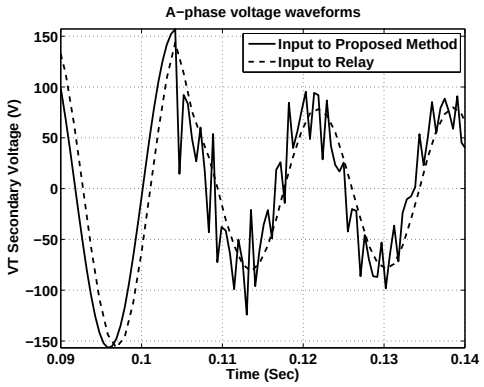
Based on the above rationale, a variety of fault-voltage waveforms were analyzed using the following methods:

1) As mentioned before, a traditional relay receives samples at its designed sampling rate (16 samples/cycle, or 960 Hz is considered in this paper). The analog waveform, therefore, needs to be filtered to avoid aliasing. For a sampling rate of 960 Hz, the cut-off frequency of the low-pass anti-aliasing filter needs to be 480 Hz or lower. Since we did not have the hardware set-up to model the traditional relay this way, we employed an alternate method: Digital waveforms were created using an extremely high sampling rate of 96 kHz (1600 samples/cycle) by selecting an appropriate time-step in the simulation. This would ensure practically zero aliasing as indicated in Fig. 1 (b). These waveform-samples were digitally filtered using a second-order Butterworth low-pass filter with a cut-off frequency of 240 Hz, down-sampled to 16 samples/cycle, and processed with DFT to estimate the phasor value of the fundamental. This process will effectively model the traditional relay using an analog second-order Butterworth anti-aliasing filter with cut-off frequency of 240 Hz, and using $f_s = 960$ Hz. Cut-off frequency lower than $f_s/2 = 480$ Hz was chosen because the second-order filter does not have a very sharp cut-off.
2) Waveform was oversampled at $f_s = 48$ kHz and directly processed with the DFT – no anti-aliasing filter was assumed. This models the proposed approach.

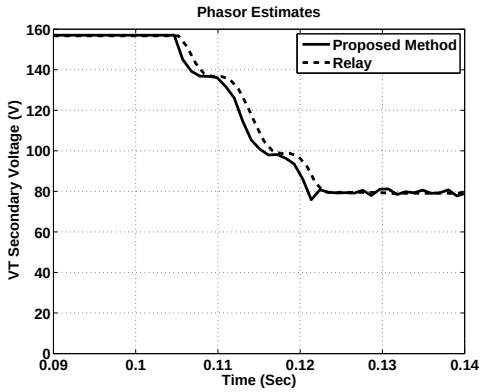
The DFT algorithm was coded using MATLAB®. The phasor estimates using the above two approaches were compared for a very comprehensive array of fault waveforms.

III. Simulation Results

First, to illustrate the effect of aliasing on the phasor estimates, we selected $2\times$ oversampling, i.e. $f_s = 960$ Hz$\times 2 = 1.92$ kHz. Fig. 1(b) shows substantial signal energy above $1.92/2 = 0.96$ kHz. With this sampling rate, Fig. 2(a) shows the input waveforms to the relay (filtered) and to the proposed method (unfiltered), and Fig. 2(b) shows the



(a)



(b)

Fig. 2. Phasor estimation with a traditional relay and with the proposed approach for sampling rate of 1.92 kHz.

phasor estimates; both referred to the secondary of the voltage transformer (VT). There is obvious discrepancy in the phasor estimates. Fig. 3 shows the results for $f_s = 48$ kHz, i.e. $50\times$ oversampling. The phasor estimates of both signals in Fig. 3(a), shown in Fig. 3(b), are practically the same, except for the one-cycle transition period from the pre-fault to fault condition. It can also be observed that the phasor estimation using the proposed approach is faster, as it avoids the delay associated with the anti-aliasing filter.

The transient content in a fault waveform can vary with the fault location, fault instant, fault type, pre-fault conditions and fault resistance. Therefore, it is important to test the chosen sampling rate with respect to these various conditions. Therefore, the sampling rate of 48 kHz was applied to voltage waveforms corresponding to such conditions, and was found to provide practically the same phasor estimates as from the traditional relay. Each type of fault (LLL, LL, LG, LLG) was created at 5%, 50%, and 95% distance from the sending end of the simulated transmission line. Each fault was created at near zero-crossing of the voltage waveform, around the peak of the waveform, and at an instant half-way between. Fault resistances up to 50 Ω were considered for faults involving ground, and up to 10 Ω for other types. These values are higher than the typical fault resistance values quoted in [5]. Fig. 4 shows the results for a LG fault at 100 km from the sending end. Fig. 5 shows the results for a LLL fault at 150 km from the sending end. Both these faults take place at a point between the zero-crossing and the peak of the voltage waveform. The LLL fault was created with a pre-fault angle difference between two ends of the transmission line being 18°. It can be seen that $f_s = 48$ kHz gives satisfactory results in both cases. This was true for all the cases tested.

It should be mentioned here that some lower sampling rates also gave good results. We tried the three most commonly found audio-band sampling rates: 48 kHz, 24 kHz, and 18 kHz. There was practically no difference in the results obtained with 24 kHz and 48 kHz for the cases we investigated. There was, however, a perceptible difference with a sampling rate of 18 kHz. It was decided to select $f_s = 48$ kHz to include a safety margin.

It is also important to mention here that the proposed method does not require performing the DFT after every new sample enters the data-window. At the proposed rate, that would mean 800 phasor-estimates per cycle, which is not necessary. The results presented here were obtained by performing DFT only 16 times per cycle, just like a traditional relay. However, the data-window with the proposed method has 800 samples as compared to 16 samples in the traditional relay. Equation (2) shows the DFT process.

$$V = \frac{2}{N}\sum_{n=0}^{N-1} v(n)e^{-j2n\pi/N} \tag{2}$$

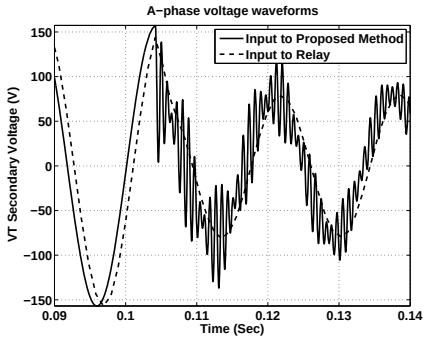
In (2), V is the phasor estimate of the fundamental, N the number of samples in the data-window, and $v(n)$ is the value of the n^{th} data-sample. We use (2) with a sliding data window. With a sampling rate of 16 samples per cycle, DFT will be performed after every new sample enters the data window. In our case, we wait for $800/16 = 50$ new samples to enter the data window before we perform DFT. With 16 samples/cycle, N in (2) equals 16; in our case it equals 800.

For the CPU, the extra calculation burden comes from the increased window size (800 v/s 16 samples). In (2), the terms inside the summation symbol constitute one real term ($v(n)$), and the other complex term (exponential). This means there are two Multiply and one Add operations to implement the term inside the summation symbol once. For the larger window, ($N = 800$), the total MAC (Multiply-Accumulate) operations required are $800 \times 2 = 1600$ instead of $16 \times 2 = 32$ for the smaller window ($N = 16$). The added calculation burden is therefore $1600 - 32 = 1568$ MAC operations. If we assume the CPU/DSP effectively executes one MAC instruction per clock cycle, a 100 MHz processor (as an example), increases the computation time to $(1600 - 32)/(100 \times 10^6) = 15.68$ μs for calculation of (2). Since we calculate the phasor value only 16 times per cycle with the proposed method, the time interval between successive calculations of (2) is $1/60/16 = 1042$ μs for a 60 Hz system. Thus, the added calculation time will not affect the real-time implementation at all. With current digital hardware technologies that use a much higher processor speed this is even more of a non-issue.

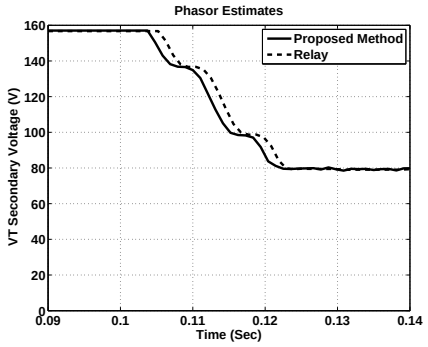
The increase in the VA burden of the relay due to the increased window size is unlikely to be significant. It is likely that the existing CPU/DSP in the digital relay can

accommodate the increased computation due to the increased window size, since it is relatively small. In this case there would be no additional power consumption. Otherwise, newer CPU/DSP chips which can accommodate the increased computation typically consume less than 1 W. The major part of the VA burden is due to the Operational Amplifiers used in ADCs rather than the chip.

The cost of commercially available ADC chips employing the chosen sampling rate is typically less compared to the cost of an analog anti-aliasing filter. Numerical relays require multiple anti-aliasing filters, depending on the number of input channels used. Removal of these filters, therefore, will result in saving in cost as well as saving in board-space.



(a)

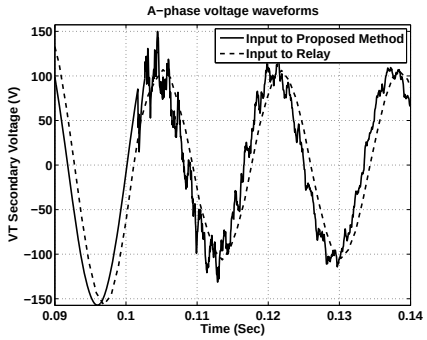


(b)

Fig. 3. Phasor estimation with a traditional relay and with the proposed approach for sampling rate of 48 kHz.

IV. Conclusion

This paper investigates the possibility of removing the analog anti-aliasing filter from the traditional digital relay without sacrificing the quality of the phasor estimation performed by the relay. Oversampling of the analog waveform is used to achieve the objective. Using extensive testing on fault waveforms generated using PSCAD/EMTDC®, a suitable oversampling rate is suggested. It is shown that the performance of the traditional relay with the anti-aliasing filter and the performance using the proposed approach are *equivalent*. This indicates that the approach is technically sound. The potential advantage of this approach is savings in cost and space. Oversampling also provides greater design flexibility for low cost digital filters that can provide a better performance



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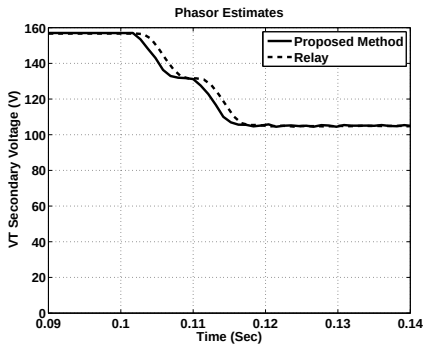
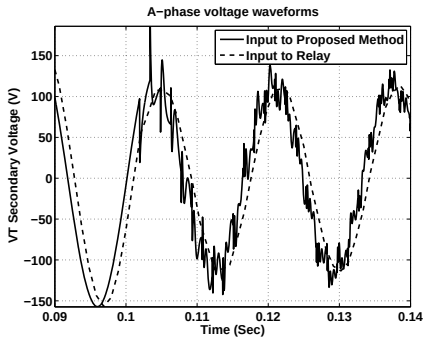


(b)

Fig. 4. Phasor estimation with a traditional relay and with the proposed approach for LGF at 100 km from sending end.



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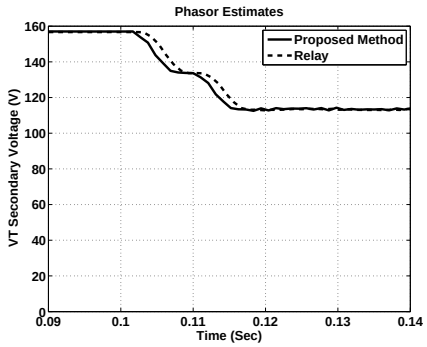

(b)

Fig. 5. Phasor estimation with a traditional relay and with the proposed approach for LLLF at 150 km from sending end.

than traditional relays. Our future efforts will be aimed at designing such digital filters.

APPENDIX

Transmission Line - 225 km:
Positive sequence impedance: 0.0358 + j0.4918 Ω/km
Zero sequence impedance: 0.352 + j1.3456 Ω/km
Positive sequence capacitive susceptance: 6.841 μS/km
Zero sequence capacitive susceptance: 4.24 μS/km
Sending End Source:
Positive sequence impedance: 5 + j27.7095 Ω
Zero sequence impedance: 10.5 + j56.55 Ω
Receiving End Source:
Positive sequence impedance: 0.6 + j9.3119 Ω
Zero sequence impedance: 1.3 + j18.85 Ω

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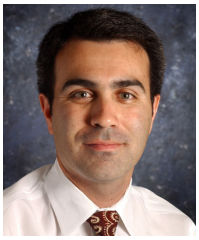

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