MOTOROLA

Chip Errata
DSP56302 Digital Signal Processor
Mask: 0F47S, 1F47S

General remark: In order to prevent the usage of instructions or sequence of instructions that do not operate correctly, the user is encouraged to use the "lint563" program to identify such cases and use alternative sequences of instructions. This program is available as part of the Motorola DSP Tools CLAS package.

ERRATA

Errata Description	Applies to Mask
1. Description: JTAG related errors a. The reset value of the JTAG Instruction Register is 1 (SAMPLE/PRELOAD) instead of 2 (IDCODE), which is required by the standard. Workaround: Not available b. The user may not write the OnCE™ Command Register (OCR) when in a daisy-chain configuration. Workaround: Write OCR register while keeping all the other devices in BYPASS. c. The data in the $\overline{BL}$ pin, Port A data bus D[23:0], and the HI32 pins HP[50:0] might be erroneous in EXTEST JTAG mode. Workaround: Do not use EXTEST for these pins. d. After exiting EXTEST, a false debug request might be received. Workaround: After exiting EXTEST, assert $\overline{TRST}$ pin (Test Reset) before normal activity.	0F47S 1F47S
2. Description: The DSP56302 cannot work with a low frequency crystal (less than 500 KHz) connected as its clock source between EXTAL and XTAL pins. Workaround: Not available	0F47S 1F47S

Errata Description	Applies to Mask
3. Description: If any DMA channel is active and a second DMA channel is enabled by writing DE = 1 and TM = 011 to its control register, and the next instructions cause "transfer stall" (see Appendix B-3.4.2 in the DSP56300 core specification) or "conditional transfer interlock" (see paragraph B-3.5.1 in the DSP56300 core specification), then the second DMA channel does not start data transfer. Workaround: Insert one NOP instruction between the DMA control register write and the sequence causing the "transfer stall" or "conditional transfer interlock". Do not place a write instruction to the DMA control register with DE = 1 and TM = 011 as a second word of a fast interrupt routine.	0F47S 1F47S
4. Description: Two sequential 1-cycle writes to the same peripheral do not work properly. Workaround: Not available	0F47S 1F47S
5. Description: When external bus activity is disabled (OMR[4] is set) and there is a contention between the DMA and core access to internal memory (access to the same 256-word bank), the DMA does not function properly. Workaround: Do not disable external bus activity (do not set OMR[4]) if the DMA will be used.	0F47S 1F47S
6. Description: When the stack extension is enabled and a nested DO loop with consecutive LAs ends causing SP to return to 0, a stack extension operation which fills the HW stack is wrongly executed (but no stack error occurs), causing EP to be decremented under its lowest permitted value. If this section of the memory belongs to another program task, damage will be caused because of stack extension operation that will overwrite these two memory locations (EP-1 and EP-2). Workaround: Any of the following alternatives can be used: a. Guarantee that EP-1 and EP-2 memory locations are not used by any task. b. Separate the two consecutive LAs by one instruction. c. Push a dummy value onto the stack before the nested DO loop.	0F47S 1F47S

	Errata Description	Applies to Mask
7.	Description: The STOP instruction does not work properly. Workaround: Not available	0F47S 1F47S
8.	Description: The $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, PINIT/$\overline{\text{NMI}}$, HCLK, and $\overline{\text{RESET}}$ pins do not have the proper 5 volt protection. Workaround: Not required.The pins function correctly as specified. There is no significant reliability degradation expected. It is recommended that the system apply only 3.3 volt levels to these pins if possible	0F47S 1F47S
9.	Description: Stack extension mechanism does not work properly if a conditional jump or branch to subroutine is used. Workaround: For the proper operation, the following instructions should not appear immediately after conditional jump or branch to subroutine: XY Memory Data Move (A-6.76) X Memory Move (A-6.71) Y Memory Move (A-6.73) Long Memory Data Move (A-6.75) Immediate Short Data Move (A-6.68) Register to Register Data Move (A-6.69) Address Register Update (A-6.70) X Memory and Register Data Move (A-6.72) Y Memory and Register Data Move (A-6.74) Arithmetic Instructions that allow Parallel Moves listed above IFcc and IFcc.U (A-6.41) Note: For this workaround, any of the listed above instructions should not be the first instruction of interrupt service routine.	0F47S 1F47S
10.	Description: When the DMA channel is enabled in triggered by request mode and the core is in the WAIT state, a false DMA data transfer might occur (e.g., one DMA request might cause two data transfers instead of one). Workaround: Not available	0F47S 1F47S

Errata Description	Applies to Mask
11. Description: XY Memory Data Move does not work properly if X-memory move destination is internal I/O and Y-memory move source is a register used as destination in the previous or next adjacent move from non Y-memory. This is not a bug, but a documentation update. Any of the following alternatives can be used: a. Separate these two consecutive moves by any other instruction. b. Split XY Data Move to two moves.	0F47S 1F47S
12. Description: Expansion Port does not provide proper Dynamic RAM support. Workaround: Not available	0F47S 1F47S
13. Description: All external memory accesses via Expansion Port cannot be performed if amount of wait states (programmed in BCR register) is less than four. Workaround: Use four or more wait states.	0F47S 1F47S

Errata Description	Applies to Mask
14. Description: A change-of-flow instruction that appears at LA-1 or LA-2 (or a two-word change-of-flow instruction at LA-3) while stack extension is enabled may cause improper operation if the preceding instruction activates the stack. For example, the following sequences may generate incorrect results: a. Example 1 DO #N,LABLE ... MOVE SSH,N3 ; stack activating instruction JSR R1 ; LA-1 NOP ; LA LABLE b. Example 2 DO #M,LABLE1 DO #N,LABLE2 ... NOP ; stack activating instruction LABLE2 JSR R1 ; LA-1 NOP ; LA LABLE1 Workaround: For proper operation the following should be guaranteed: a. Stack activating instruction does not appear immediately before the restricted change of flow instruction described above. Note: For nested DO-loops, any instruction at LA is a stack activating instruction. b. Interrupt service routines should not include more than fifteen stack pushes and pops.	0F47S 1F47S

Errata Description	Applies to Mask
15. Description: When the DMA performs external memory accesses with a priority higher than the core, and both continuous mode and interrupt enable bits are set in the channel's control register, then the DMA interrupt may not occur if the core performs external memory access immediately after enabling the DMA channel (setting DE = 1). Workaround: In this scenario, use any of the following alternatives: a. Do not set continuous mode. b. Use dynamic DMA-core priority. c. Guarantee that the core will perform at least two instructions fetched from internal memory immediately after setting of the DE.	0F47S 1F47S

16. Description:
 	
If stack extension is enabled, and a MOVE to/from SSH is followed by Address Generation Interlock of Type0, then improper operation may occur. For example, the following sequence may generate incorrect results:
 	
MOVE SSH,A
MOVE #0,R7
MOVE A,X:(R7)
 	
Workaround: After a MOVE to/from SSH instruction, use any instruction sequence that does not cause Address Generation Interlock of Type0.
 	
Note: Make sure that no interrupt service routine starts with an Address Generation Interlock of Type0.
	0F47S
	1F47S

17. Description: When the chip is powered up with PLL enabled (PINIT=1), the skew between EXTAL and CLKOUT after the PLL locks cannot be guaranteed at high frequency (over 50 MHz, not 100% tested). Workaround: If skew between EXTAL and CLKOUT is needed, power up with PINIT=0, and then enable the PLL through software.	0F47S 1F47S

Errata Description	Applies to Mask
18. Description: After the HC bit is set by the host processor writing to the HCVR, the Host Command interrupt is executed as defined by the specification. However, if the host processor performs a read access from the HI08 port concurrently with the servicing the Host Command interrupt request by the DSP core, the HC bit in the ISR may remain set even after the HCP status bit in the HSR is cleared. Workaround: Either of the following alternatives may be used: a. Do not allow the host processor to read any HI08 register while the DSP is servicing the Host Command interrupt request. b. Use a handshake protocol with host flags instead of polling the HC bit in the ISR. A host flag (in the HCR) should be changed by the DSP (e.g., using the BCHG instruction) while performing the Host Command interrupt service routine. The host processor should read the corresponding host flag (in the ISR) before writing a new Host Command to the HCVR and then poll this flag for the change. When the flag is changed, signifying that the DSP has serviced the HC interrupt request, the host processor may clear the HC bit or send a new Host Command.	0F47S 1F47S
19. Description: If the DMA channel performs non-zero wait state data accesses to/from external memory and the DMA interrupt is enabled, a false interrupt may occur in addition to the correct one. Workaround: Ensure that the channel's DTD status bit in the DSTR register is set before jumping to the interrupt service routine (i.e., the interrupt is correct only when DTD is set). Example: ORG P:I_DMA2 JSSET #M_DTD2,X:M_DSTR,ISR_ ; ISR_ is interrupt service routine label ; for DMA channel 2	0F47S 1F47S
20. Description: Normally, if the PLL disabled, the PCAP pin may be connected to V_{CC}, to Ground, or be left floating. However, this device has a latchup sensitivity on the PCAP pin. Workaround: Do not connect the PCAP pin to Ground. If the PLL is not being used, PCAP may be connected to V_{CC} or be left floating. There is no possibility of latchup if a capacitor is the only connection to PCAP.	0F47S 1F47S

Errata Description	Applies to Mask
21. Description: A one word conditional branch instruction at LA-1 is not allowed. This is not a bug, but a documentation update.	0F47S 1F47S
22. Description: Trace mode (TME bit is set in OSCR) does not work properly during REP instruction execution. Workaround: Host debugging software should disable tracing during REP instruction execution and enable it only after the whole REP cycle is complete. If the debugging software does not disable tracing during REP instruction execution, the user must ensure that programs do not enter the trace mode while executing a REP instruction.	0F47S 1F47S
23. Description: When using the 5 V tolerant pins HREQ/TRQ, HACK/RRQ, TXD, $\overline{DE}$ in open drain mode, the chip clamps the voltage at the pin to about V_{CC} + 0.4 V. Workaround: Not available.	0F47S 1F47S
24. Description: If the chip is in the Debug mode and the $\overline{RESET}$ pin is asserted to bring the chip into Normal mode without asserting $\overline{TRST}$ at the same time, the chip status will continue to be read as “Debug” mode instead of the expected “User” mode, when the status is read afterwards through the JTAG port. Workaround: Assert the $\overline{TRST}$ pin while asserting the $\overline{RESET}$ pin.	0F47S 1F47S
25. Description: If the chip is in the Debug mode and the $\overline{TRST}$ pin is asserted, the chip status will show the chip status as “User” mode instead of the expected “Debug” mode, when the status is read afterwards through the JTAG port,. Workaround: Execute the following JTAG commands before reading the JTAG status: a) Enable OnCE b) DEBUG request Afterwards, the status bits will reflect the actual status of the chip and the $\overline{DE}$ pin will acknowledge “re-entering” the Debug mode.	0F47S 1F47S

Errata Description	Applies to Mask
26. Description: When SCI transmitter is used in Synchronous mode, the last bit of the transmitted byte might be truncated to the half of the serial cycle. Workaround: Not available.	0F47S 1F47S

NOTES

1. An over-bar (i.e., $\overline{xxxx}$) indicates an active-low signal.
2. The letters seen to the right of the errata tell which DSP56302 mask numbers apply.
3. The Motorola DSP website has additional documentation updates that can be accessed at the following URL:

   http://www.mot.com/SPS/DSP/home/eng/tec/doc_update.html

   Information contained in the addendum to the DSP56301 data sheet applies to all members of the DSP56300 core family, as applicable (i.e, references to the HI32 port do not apply to the DSP56302 and DSP56303).

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