DSP56302

Advance Information

DSP56302 Evaluation Module

The DSP56302 Evaluation Module (DSP56302EVM) is designed as a low-cost platform for developing real-time software and hardware products to support a new generation of applications in wireless, telecommunications, and multimedia products using multi-line voice / data / fax processing, videoconferencing, audio applications, control, and general digital signal processing. The user can download software to on-chip or on-board RAM, then run and debug it. The user can also connect hardware, such as external memories and A / D or D / A converters, for product development. The 24-bit precision of the DSP56302 Digital Signal Processor (DSP) combined with the on-board 32 K of external SRAM and Crystal Semiconductor's CS4215 stereo, CD-quality, audio codec makes the DSP56302EVM ideal for implementing and demonstrating many communications and audio processing algorithms, as well as for learning the architecture and instruction set of the DSP56302 processor. **Figure 1** shows the functional block diagram for the DSP56302EVM.

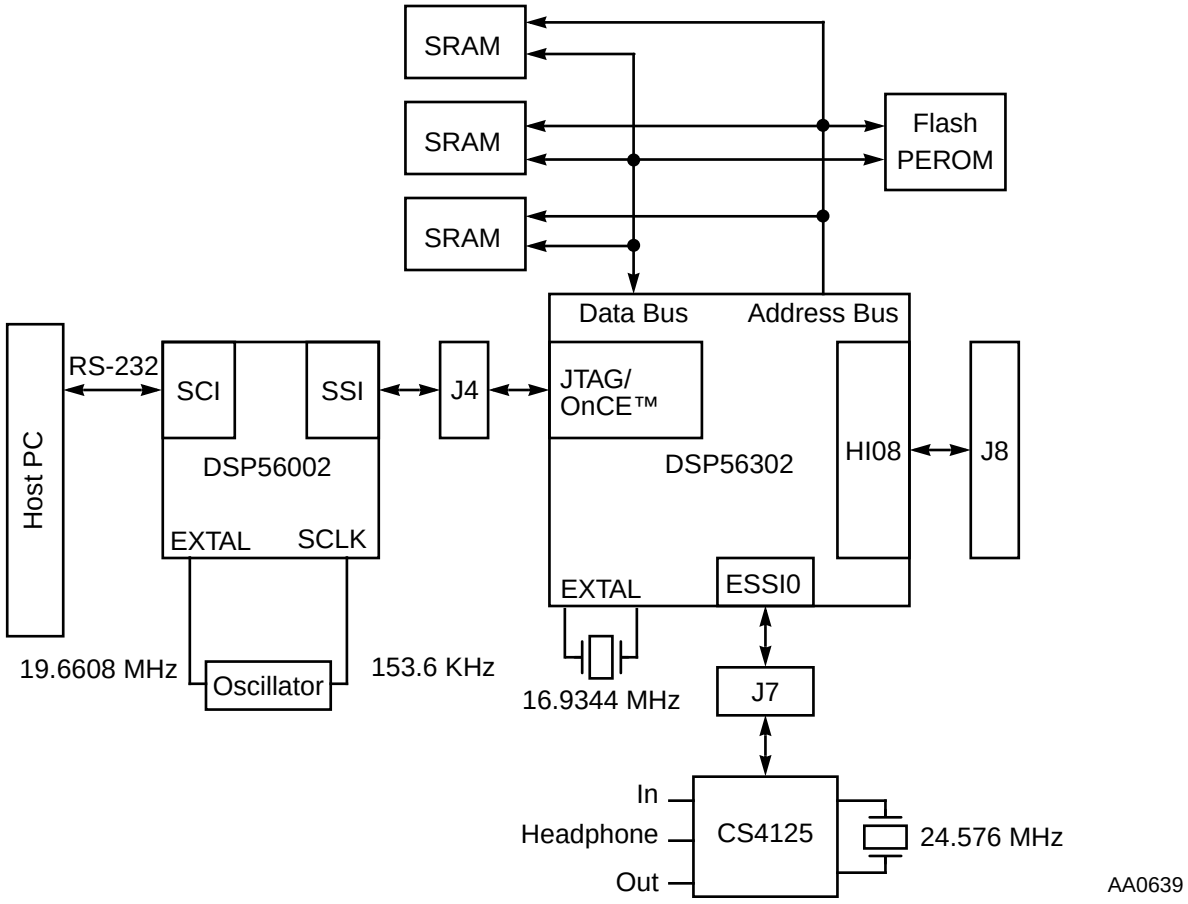

Figure 1 DSP56302EVM Functional Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preliminary Information

Features

Hardware

- 24-bit DSP56302 Digital Signal Processor
  - High Performance DSP56300 Core
    - 66/80 Million Instructions Per Second (MIPS) with a 66/80 MHz clock
    - Object-code compatible with the DSP56000 core
    - Highly parallel instruction set
    - Fully pipelined 24 × 24-bit parallel multiplier-accumulator
    - 56-bit parallel barrel shifter
    - 24-bit or 16-bit arithmetic support under software control
    - Position Independent Code (PIC) Support
    - Unique DSP addressing modes
    - On-chip memory-expandable hardware stack
    - Nested hardware DO loops
    - Fast auto-return interrupts
    - On-chip concurrent six-channel DMA controller
    - On-chip Phase Lock Loop (PLL)
    - On-Chip Emulation (OnCE™) module
    - JTAG port
    - Address tracing mode reflects internal program RAM accesses at external port
  - On-Chip Memories
    - Program RAM, Instruction Cache, X data RAM, and Y data RAM size is programmable:

Instruction Cache	Switch Mode	Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size
disabled	disabled	20480 × 24-bit	0	7168 × 24-bit	7168 × 24-bit
enabled	disabled	19456 × 24-bit	1024 × 24-bit	7168 × 24-bit	7168 × 24-bit
disabled	enabled	24576 × 24-bit	0	5120 × 24-bit	5120 × 24-bit
enabled	enabled	23552 × 24-bit	1024 × 24-bit	5120 × 24-bit	5120 × 24-bit

    - 192 × 24-bit bootstrap ROM

- Off-Chip Memory Expansion
  - Data memory expansion to two memory spaces of 256 K × 24-bit words
  - Program memory expansion to one memory space of 256 K × 24-bit words
  - External memory expansion port
  - Four chip-select logic lines for glueless interface to SRAMs and SSRAMs
  - On-chip DRAM controller for glueless interface to DRAMs
- On-Chip Peripherals
  - Enhanced DSP56000-like 8-bit parallel Host Interface (HI08)
  - Two Enhanced Synchronous Serial Interfaces (ESSI)
  - Serial Communications Interface (SCI) with baud rate generator
  - Triple timer module
  - Up to thirty-four programmable General Purpose Input / Output (GPIO) pins, depending on which peripherals are enabled
- Reduced Power Dissipation
  - Very low power CMOS design
  - Wait and Stop low power standby modes
  - Fully-static logic, operation from the device maximum frequency down to DC

- 32 K × 24-bit fast Static RAM for expansion memory
- 64 K × 8-bit Flash PEROM for stand-alone operation
- 16-bit CD-quality audio codec
  - Two channels of 16-bit Analog-to-Digital (A / D) conversion
  - Two channels of 16-bit Digital-to-Analog (D / A) conversion
  - Software-selectable 8-bit and 16-bit data formats, including μ-law and A-law companding
  - Stereo jacks for audio input, output, and headphones
- Command Converter
  - DSP56002 for high-speed OnCE / JTAG command conversion software
  - JTAG connector for use with the Application Development System (ADS) command converter card
- Connectors
  - Host-to-ISA bus connector
  - Port A connector
  - ESSI0, ESSI1, and SCI connector

Software

- Motorola's DSP56xxx cross assembler
  - Produces DSP56302 binary code from source code using labels, sections, and macro definitions incorporating the DSP's complete instruction set, all addressing modes, and all memory spaces
  - Offers macros, expression evaluation, and functions for strings, data conversion, and transcendentals
  - Creates reports for cross-references, instruction cycle count, and memory usage
  - Provides extensive error checking and reporting
- Domain Technologies debug software with Windows-based user interface
  - Symbolic debugging
  - Windows for data, code, DSP registers, commands, peripherals, etc.
  - Data and registers displayed in fractional, decimal, or hexadecimal format
  - Graphical display of memory segments
  - Up to eight simultaneous software breakpoints
  - Built-in-line assembler and disassembler
- Demonstration software and example pass-through code
- Self-test files—executable and source code (Flash PEROM is preprogrammed with self-test and audio echo software.)

User Requirements

The user must provide the following:

- Power supply (7–9 V AC or DC with 2.1 mm power connector)
- RS-232 cable (DB9 male to DB9 female)
- Audio source, headphones, and a cable with 1/8-inch stereo plugs
- IBM PC compatible computer (386 class or higher) running Windows 3.1 (or higher) with an RS-232 serial port capable of 9,600–57,600 bit-per-second operation, 4 Mbytes RAM, 3-1/2 inch diskette drive, hard drive with 4 Mbyte of free disk space, and a mouse

SUPPORTING DOCUMENTATION

The first three documents listed in **Table 1** are required for a complete description of the DSP56302 and are necessary to design properly with the part. The fourth and fifth documents provide a description of the DSP56302EVM, including installation and use. These documents are provided with the DSP56302EVM. Additional copies are available from one of the following locations (see back cover for detailed information):

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

The DSP56302EVM can be ordered by the number listed below from the same locations.

Table 1 Documentation List

Document Name	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD
DSP56302 User's Manual	Detailed functional description of the DSP56302 memory configuration, operation, and register programming	DSP56302UM/AD
DSP56302 Technical Data	DSP56302 features list and physical, electrical, timing, and package specifications	DSP56302/D
DSP56302EVM Product Information	Overview description of the DSP56302EVM, including block diagram and list of features	DSP56302EVMP/D
DSP56302EVM User's Manual	Detailed functional description of the DSP56302EVM, including requirements, installation, and general operating guidelines	DSP56302EVMUM/AD
DSP56302EVM	DSP56302 Evaluation Module kit with hardware, software, and documentation	DSP56302EVM

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