DSP56302 Processor General Description

Reading

Chapter 1 Core Description of *Motorola DSP56300 Family Manual*
Chapter 3 Data Arithmethic Logic Unit of *Motorola DSP56300 Family Manual*

Introduction

There are two general types of architectures for processors: Harvard and Princeton.

Figure: Harvard architecture (2 memories, 2 busses)

Figure: Princeton architecture (1 memory)

The DSP5630*x* device is based on a modified Harvard architecture which includes an additional data memory and associated bus. This architecture incorporates the important feature of duality which facilitates many Communications and DSP applications such as

- complex numbers where data consist of real and imaginary components (I- and Q- channels)
- audio applications requiring left and right channel processing [digital audio (stereo)]

DSP56K Core

All DSP5630*x* devices are based on the DSP56300 core (See Chapter 1 of the *DSP56300FM*). The individual family members are designed with different peripherals and memory configurations so as to better suit the target application. The major components of the DSP56300 core are

- Three independent execution units
  - Data Arithmetic Logic Unit (ALU) – performs all arithmetic and logical operations on data operands
  - Address Generation Unit (AGU) – performs effective address calculations to address data in memory
  - Program Control Unit (PCU) – performs instruction prefetch, instruction decoding, hardware DO loops, and exception processing
- Four independent 24-bit data busses
  - X Data Bus (XDB)
  - Y Data Bus (YDB)
  - Program Data Bus (PDB)
  - Global Data Bus (GDB)
- Three independent 24-bit address busses (capable of accessing 16M of memory)
  - X address bus (XAB)
  - Y address bus (YAB)
  - Program address bus (PAB)
- Highly parallel instruction set with unique addressing modes

DSP56300 Architecture Introduction

Motorola Training Notes 1-6 through 1-14

